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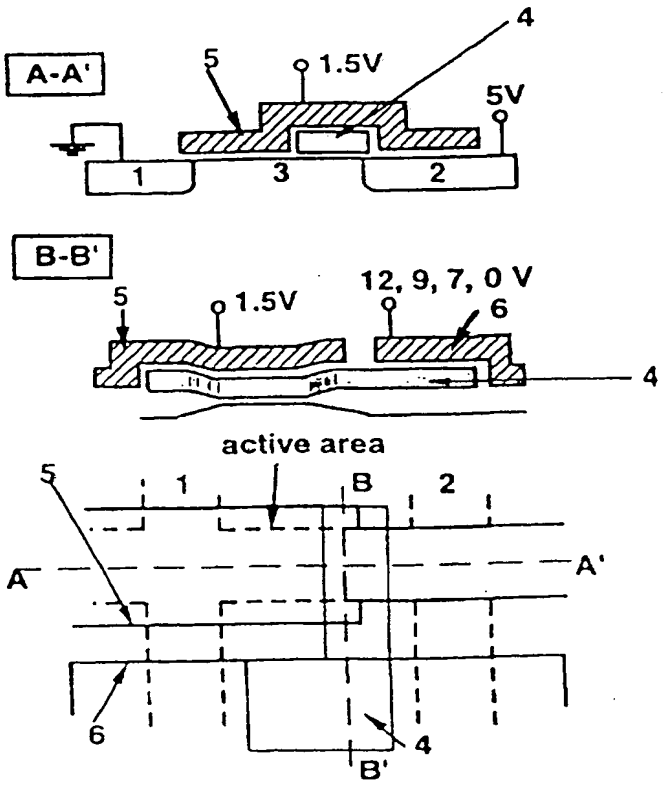
(54) Title: A DEVICE AND METHOD FOR MULTI-LEVEL CHARGE/STORAGE AND READING OUT

(57) Abstract

The present invention discloses a memory device having memory cells capable of storing three or more charge levels in said memory cell. The cells can be programmed according to a method including a single pulse charge level injection mechanism in said cells. The method does not require a program verify scheme, permits increased speed during programming, and reduces the area necessary for storing one bit of information. The memory device of the present invention further includes information write or storage or programmation means, information erase means and information read-out means. Another object of the present invention is to provide a method and a circuit that implements said method for determining the charge level of a memory cell having t possible levels (t being larger than or equal to three). The circuit measures the similarity of the memory cell drain current with the drain current of each of n references, determines the one reference which is the most similar to the memory cell and thereby identifies the charge level of said memory cell.



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A DEVICE AND METHOD FOR MULTI-LEVEL CHARGE/STORAGE AND READING OUT

FIELD OF THE INVENTION

The present invention relates to a non volatile memory device for multi-level charge storage. More in particular a device and a method for multi-level charge storage and an apparatus and a method for reading out said device is disclosed.

BACKGROUND OF THE INVENTION

Non-volatile semiconductor memory devices are an important class of solid-state memory devices. A particular type of non-volatile semiconductor memory devices are flash EEPROM devices. The primary mechanism by which data are stored in a non-volatile memory device is by access to a memory cell. The demand for high-density Flash EEPROM memory devices in portable computing and telecommunication applications stimulates continuous efforts on flash EEPROM memory cell size scaling. In order to further increase the storage capability of Flash memory devices, Multi-Level Charge Storage (MLCS) techniques have been developed. These techniques allow furthermore to reduce the cost per bit of information of flash eeprom non-volatile memory devices.

Typically, a MLCS memory device is configured such that 2^n different charge levels, corresponding to threshold voltage levels, can be stored in one memory cell and the current corresponding to these different threshold voltage levels can be read-out. Thus, storage and read-out of n bits of data (with n being larger than or equal to two) in a single memory cell can be achieved. The cost per bit of

information with MLCS techniques is reduced as a number related to 1/n.

Multi-level storage or write or progammation circuits and techniques, and read-out circuits and techniques have been disclosed. U.S. Patent No 5,043,940 of Harrari discloses a split-channel EEPROM device that can be programmed in more than two programmable threshold states. U.S. Patent No 4,771,404 of Mano et al. discloses a memory device which has memory cells capable of storing ternary or more information. This memory device includes a multilevel detector for detecting the information of the memory cells at one time and a reference generator for generating reference levels therefor. U.S. Patent No. 5,163,021 of Mehrotra et al. discloses improvements in the Circuits and Techniques for read, write and erase of Multi-State EEPROM memory devices, the improved circuits making the reading relative to a set of threshold levels as provided by a corresponding set of reference cells. U.S. Patent No 4,415,992 discloses a read-out scheme for discriminating n charge levels of a memory cell in which (n-1) comparators and (n-1) voltage references are used in parallel to determine the charge level of the memory cell. Additional decoding logic is required to translate the outputs of the comparators into bits. A total of (2n - 1) different voltage amplitudes are necessary, and have to be implemented on chip. Other multilevel storage memory devices and programming methods have been disclosed in WO95/34074, US 5422845 and WO95/34075.

A main disadvantage applying to the memory devices disclosed in the prior art is that they, in functioning, make use of a bit-by-bit program verification procedure. This procedure suffers from trade-offs between accuracy of the stored levels and programming speed. Consequently the programming operation slows down. Moreover, the chip implementation of said verification procedure increases the chip dimensions. Furthermore, the memory devices reported in

the prior art employ read-out circuits based on a plurality of comparators and decoding logic which not only increase the complexity of the memory device but also enlarge the chip dimensions.

The prior art memory cells for multi-level charge storage employ programming methods based on either Fowler Nordheim Tunneling (FNT) or Channel Hot Electron (CHE) injection. The prior art multi-level programmming methods utilize a 'program verify scheme' comprising the following common steps:

(1) A programming pulse of typically 100 microseconds to 1 millisecond duration is applied to the memory cell to be programmed;
(2) The drain current of the memory cell to be programmed is sensed and presented to a comparator circuit which also has presented to it the current of a reference current source corresponding to one of the multilevel charge levels to which the cell has to be programmed;
(3) If the current of the memory cell and the current of the reference current source match, then the cell is in the correct state and no further programming is required. If however the currents do not match, then steps (1) and (2) are repeated.

The prior art programming methods fail to disclose a MLCS method characterized by high programming speed and small chip size required to implement the memory device. Since according to the prior art programming methods several iterations of the programming steps are required, and after each step a sensing step is required in order to accurately program the cell to the intended charge level, the speed of the entire programming operation is significantly compromised. The speed furthermore is a function of the particular charge level that has to be programmed. These disadvantages considerably decrease the data throughput of

the memory device. The second problem has to do with silicon area consumption, since the silicon implementation of the 'program verify scheme' increases the chip size.

SUMMARY OF THE INVENTION

It is an object of the present invention to disclose a memory device having memory cells capable of storing three or more charge leves in said memory cell. The memory cells can be programmed according to a method including a single pulse charge level injection mechanism in said cells. The method does not require a charge level verify scheme, permits increased speed during programming, and reduces the area necessary for storing one bit of information. The speed of said programming mechanism is at least two orders of magnitude faster than other multi-level programming mechanisms described in the prior art. The memory device of the present invention further includes information write or information storage or information programmation means, information erase means and information read-out means. It is to be understood in the sequel that the terms writing or storage or programming specify equivalent methods or circuits or means.

Yet another object of the present invention is to provide a method and an apparatus and circuit that implements said method for reading out the charge level of a memory cell having t possible states (t being larger than or equal to three). The circuit measures the similarity of the drain current of the memory cell with the drain current of each of m references, stored in dummy cells, determines the one reference which is the most similar to the memory cell and thereby identifies the charge level of said memory cell.

In one aspect of the present invention, a memory device adapted for multi-level charge storage is disclosed. The

memory device comprises a plurality of flash eeprom memory cells and further comprises means for programming said charge levels and readout means for parallel outputting binary data corresponding to said charge levels stored in said cells. By preference the memory cells of the memory device comprise in a semiconductor substrate a source region, a drain region, and a channel region. The memory cell further comprises a floating gate, said floating gate including first and second floating gate portions, said first portion extending over said channel region, said second portion extending away from said channel region. Said memory cells further include a program gate and a control gate, said program gate forming a capacitor with said second floating gate portion. The programming means of the memory device furthermore comprise means for applying a high voltage pulse with a predetermined amplitude, selected from a plurality of predetermined amplitudes and with an essentially fixed time width to said cells. Said predetermined amplitudes determine said charge levels. The charge levels correspond to different threshold voltage levels of one memory cell. The memory cells of the memory device by preference are arranged in an array with rows and columns having the drains of the cells belonging to the same column connected together whereby forming a data output line, the program gates of the cells belonging to the same column connected together whereby forming a data input line. The control gates of the cells belonging to the same row furthermore can be connected together whereby forming a word line.

In a second aspect of the present invention is disclosed a method of storing one of a plurality of charge levels in a memory cell including a source region, a drain region, a channel region and a floating gate, said floating gate including first and second floating gate portions, said first portion extending over said channel region, said second portion extending away from said channel region, said memory cell further including a program gate and a control gate,

said program gate forming a capacitor with said second floating gate portion. The method comprises the steps of applying a low voltage to said control gate; applying a voltage not greater than 5 Volt to said drain region; and applying a high voltage pulse with a predetermined amplitude, selected from a plurality of predetermined amplitudes and with an essentially fixed time width to said program gate, said predetermined amplitudes determining said charge levels. The method further comprises the step of capacitively coupling said high voltage pulse to said second floating gate portion, thereby causing a hot-electron injection towards said floating gate whereby one of the plurality of charge levels is stored in said memory cell.

In another aspect of the present invention, a method is disclosed of making uniform the electrical field stress induced by programming to different charge levels the memory cells of the array of the memory device according to the present invention. The method comprises the steps of applying a low voltage to the control gates of essentailly each of the memory cells of the array; applying a voltage not greater than 5 Volt on the drain regions of essentailly each the memory cells of the array; and applying a high voltage pulse with a predetermined amplitude and an essentially fixed time width on the program gates of essentailly each of said cells of said array; and thereafter erasing said cells.

Yet in another aspect of the present invention, a method of reading out the charge level of a memory cell of the memory device according to the present invention is disclosed. Said method comprises the steps of sensing the drain current of said memory cell; sensing the drain currents of a plurality of dummy cells; measuring the similarities between said drain current of said memory cell and said drain currents of said plurality of dummy cells whereby obtaining a plurality of intermediate voltages representing said similarities; determining the highest among said intermediate

voltages whereby identifying the dummy cell having the drain current closest to the drain current of said memory cell; and setting a predetermined voltage on one of a plurality of output terminals, said one output terminal corresponding to said dummy cell having the drain current closest to the drain current of said memory cell.

In a further aspect of the present invention an apparatus or circuit is disclosed for reading out the charge level of a memory cell. The apparatus comprises a plurality of dummy cells for delivering a plurality of reference currents ; means for reading out said reference currents and the current of said memory cell; a plurality of analogue circuits for measuring the similarity between said current of said memory cell and each of said reference currents whereby outputting a plurality of intermediate voltages representing said similarities; a decision circuit for determining the highest among said intermediate voltages whereby determining the dummy cell having the drain current with the smallest distance from the drain current of said memory cell and for setting a predetermined voltage on one of a plurality of output terminals, said one output terminal corresponding to said dummy cell having the drain current with the smallest distance from the drain current of said memory cell.

DETAILED DESCRIPTION OF THE DRAWINGS

Figure 1 shows a memory cell according to a preferred embodiment of the invention.

Figure 2 shows an array of memory cells according to a preferred embodiment of the invention.

Figure 3 shows the threshold voltages and read-out currents of cells programmed acoording to the Voltage Variant Source Side Injection methid of the present invention.

Figure 4 shows the programming characteristics of Voltage Variant Source Side Injection.

Figure 5 shows a state of the art Read-out architecture.

Figure 6 shows the working principle of the Read-out architecture according to a preferred embodiment of the invention.

Figure 7 shows the block diagram of the Read-out architecture according to a preferred embodiment of the invention.

Figure 8 shows a schematic drawing of subcircuit 400, 401, 402 and 403 of figure 7.

Figure 9 shows a schematic drawing of subcircuit 500 of figure 7.

Figure 10 shows the detailed layout of the Read-out architecture according to a preferred embodiment of the invention.

Figure 11 shows experimental results representative for subcircuit 400, 401, 402 and 403.

Figure 12 shows experimental results of the Read-out architecture according to a preferred embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

It is an object of the present invention to disclose a memory device having memory cells capable of storing three or more charge levels. The cells can be programmed according to a method including a single charge level injection mechanism

in said cells. The method does not require a program verify scheme, permits increased speed during programming, and reduces the area necessary for storing one bit of information. The speed of the programming mechanism is at least two orders of magnitude faster than other multi-level programming mechanisms described in the prior art . The memory device of the present invention further includes information write means, information erase means and information read-out means.

For the purpose of teaching only, in the following description, an implementation of the memory device and method of storing data in said memory device will be described for the case where 2^n different threshold voltage levels can be stored in a memory cell, with n=2. It is obvious that, according to the teaching of the invention, other embodiments of this invention can be configured by the person of skill in the art for n > 2, the spirit and scope of the present invention being limited only by the terms of the appended claims.

Figure 1 shows a memory cell of the memory device according to a preferred embodiment of the invention. The memory cell is a flash EEPROM cell structure implemented in a silicon substrate and comprises a source region 1, a drain region 2 and a channel region 3 therebetween. The memory cell further comprises a floating gate 4, said floating gate including first and second floating gate portions, said first portion extending over said channel region 3 with a thin oxide layer therebetween, said second portion extending away from said channel region. Said memory cell further includes a program gate 6 and a control gate 5, said program gate 6 forming a capacitor with said second floating gate portion, the control gate extending over said first portion of the floating gate. The program gate 6 forms a capacitor with the floating gate 4 with a high coupling ratio of about 50 % or more. A dielectric layer is inbetween said program gate and

said floating gate and inbetween said control gate and said floating gate. In detail the structure and a possible programming mechanism of said memory cell is disclosed in US patent 5,583,811, in US patent 5,583,810 and in the EP patent EP 0501941. The teaching of these patent applications US 5583810, US5583811, and EP 0501941 is incorporated herein by reference. This memory cell can be implemented in a 3 µm, or in a 1.2 µm, or in a 0.7 µm, or in a 0.5 µm, or in a 0.35 µm or in a 0.25 µm or in a 0.18 µm or in a 0.12 µm Complementary Metal-Oxide-Semiconductor (CMOS) silicon technology, or in any other CMOS technology with the set of layout rules and characteristic dimensions of the transistors according to the art. The memory cell according to the preferred embodiment of the present invention, when implemented in a 0.7 µm CMOS technology can have the floating gate 4, the program gate 6 and the control gate 5 being made of polysilicon material. The dielecric layer can be an oxide layer with a thickness of 25-30 nm. The thin oxide layer can have a thickness ranging from 7-9 nm. The floating gate length and the control gate length can be 0.7 µm, the width of the memory cell can be 1.8 µm.

The memory device by preference comprises an array of cells as detailed hereabove. Figure 2 illustrates an array 11 configured in accordance with one embodiment of the present invention. The array is a geometric configuration of individually addressable EEPROM cells 10 as disclosed hereabove. Thus the memory cells have a Control Gate 4, a Program Gate 6, a Drain region 2 and a Source region 1. The source 1 of all cells in the array is grounded and therefore not shown in Figure 2. The memory array 11 is arranged in m rows and z columns. Each cell belongs to one column and to one row only. The last four cells of each row are dummy cells which are used as references during the read-out operation of the memory device. Along each row, a word line is connected to all the Control Gates 5 of the cells in the row. Along each column, an output bitline is connected to all the Drains

2 of the cells. An input bitline is connected to all the Program Gates 6 of the cells in the column. Thus, the Program Gate 6 is routed in the same direction as the Drain region 2. The Control Gate 5 is routed in a direction perpendicular determined by the one of the Program Gate and the Drain. The Program Gates have to be routed by preference in parallel to the Drain regions in a Multilevel Array. In a Binary Array on the other hand, the program gates have to be routed horizontally. Since in the Voltage Variant Source Side Injection (VVSSI) multi-level programming method disclosed in the present patent application, the data to be programmed into the cells are applied on the Program Gate whereas the data to be read-out from the cells are sensed from the Drain, it follows that the Drain and the Program Gate of the cells have to be routed in the same direction in order to allow individual programming and read-out of each cell. In this Multilevel Flash EEPROM Array there are two bitlines. The output bitline, is used to read out the charge storage levels from the cells, and the input bitline is used to program the charge storage levels into the cells.

In an aspect of the present invention, a method of storing one of a plurality of charge levels in said memory cell is disclosed. A difference between the memory cells for multi-level charge storage reported in the prior art and the memory cell structure according to the preferred embodiment of the invention is that the prior art memory cells require programming schemes based on either Fowler Nordheim Tunneling (FNT) or Channel Hot Electron (CHE) injection whereas the memory cell according to this preferred embodiment of the invention employs a Voltage Variant Source Side Injection Programming method (VVSSI). This new programmation method is based on a Source Side Injection (SSI) programmation method of the memory cell. Each of the multi-level charge storage levels corresponds to a specific threshold voltage that is stored into the

Floating Gate 4 of the EEPROM memory cell. The threshold voltage of the memory cell is defined as the voltage that must be applied on the program gate 6 in order to obtain a drain current of 1 μA at a fixed value of the control gate voltage and the drain region voltage. This definition is different from other non-volatile memory cells for which the threshold voltage of the device must be defined at the control gate.

The SSI programmation method devolves on applying a high voltage to said program gate 6, thereby capacitively coupling a high voltage to said floating gate 4, applying a low voltage to said control gate 5 and applying a voltage not greater than 5 Volt to said drain region whereby causing a very high hot-electron injection towards said floating gate 4 while achieving a programming of said memory cell. VVSSI multi-level charge level programming comprises the steps of applying a single programming pulse (V_{PG}) to the program gate 6 of the cell, while the drain region 2 and control gates 4 are kept at a constant bias (V_D and V_{CG}) according to the conditions of Table 1. The programming pulse which is applied to the program gate 6 of the memory cell, has a width T of about 1 microsecond independently of the charge level to be programmed, and an amplitude which, on the contrary, is related to the charge level to be programmed as shown in Table 1. The amplitude of the programming pulse is given in Volt (V)

	Level	V_{CG} (V)	V_{PG} (V)	V_D (V)	T
VVSSI	1	1.5	7.0	5.0	1.0 µs
	2	1.5	8.0	5.0	1.0 µs
	3	1.5	12.0	5.0	1.0 µs
	0	1.5	0.0	5.0	1.0 µs
Read-out	All	4.0	0.0	2.0	

Table 1: Operating Conditions of the multi-level charge storage programmation method according to a preferred embodiment of the present invention.

The values given in table 1 are related to the implementation of the memory cell of the preferred embodiment in a 0.7 µm CMOS technology. As it is shown in table 1, the value of V_D (namely 5V) is the value of the power supply voltage of the 0.7 µm CMOS technology. If the power supply voltage is to be scaled down for other CMOS technologies as mentioned above (e.g. to 3.3 Volt for a 0.35 µm CMOS technology) the values of the different voltages reported in Table 1 can change as follows. V_D would scale down as the power supply voltage, the different V_{PG} voltages would scale down as a subtraction that is approximately equal to the double of the amount by which the power supply voltage is diminished; V_{CG} would be in the range of 0.5 - 1.3 Volts. V_{CG} for a 0.7 µm CMOS technology can be in the range of 1.5 to 1 Volt either or even lower. For instance, in the case of a supply voltage scaling from 5 to 3.3 Volts, V_D would be 3.3 Volts; V_{PG} would be about 9 Volt, 6, Volt, 5 Volt and 0 Volt for the different charge storage levels. For a 0.7 µm CMOS technology, the V_{PG} voltages as reported in table 1 can also be different. A set of programming voltages as 10 Volt, 8 Volt, 6 Volt and 0 Volt for the different charge storage levels can be used. The set of programming voltages as given in table 1 are a good compromise between the requirements of programming speed on

one hand, and accuracy of the programmed charge level on the other . Taking the pulse width of the programming pulse (V_{PG}) longer than or equal to 1 micro second ensures that all the levels are taken in the saturation region of the respective programming characteristics. Therefore, the pulse width of 1 micro second is optimal for VVSSI. The programming characteristic of a memory cell is defined as the shift of the threshold voltage of the memory cell versus the prgramming time. As the time width of the pulse is concerned, it can remain about the same with the scaling down of the CMOS technology and power supply. This is certainly an advantage, because next generation VVSSI based EEPROM memory devices would be smaller in area but not slower than the embodiment in a 0.7 µm CMOS technology.

Thus the a method of storing one of a plurality of charge levels in said memory cell utilizes a single 1 micro second programming pulse and does not require a program verify scheme to verify the accuracy of the programmed charge storage levels. In the sequel the programming performance, capability for information discrimination and endurance characteristics are explained in detail. The speed of said programming mechanism is at least two orders of magnitude faster than other multi-level programming mechanisms based on FNT described in the prior art as for instance in M. Ohkawa et al. "A 98mm^2 64Mb Flash Memory with FN-NOR type 4-level Cell", ISSCC 96, TP 2.3, pg.36. A much larger current window is the main advantage of VVSSI with respect to CHE.

40 of said EEPROM memory cells fabricated on a 6-inch silicon wafer in a 0.7 µm CMOS technology, have been programmed to the four levels according to the conditions mentioned in Table 1. The distributions of these levels, in terms of Threshold Voltage V_T and Read-Out Current I_D, have been measured and are shown in Figure 3. Also shown in figure 3 are the mean value X, and the standard deviation s

for each distribution. The cells have been measured according to the read-out conditions shown in Table 1. It is evident that the distributions are narrow and separated one from another. Thus the method of storing one of a plurality of charge levels in according to the present invention does not require a program verify scheme to verify the accuracy of the programmed charge storage levels.

An advantage of programming pulses of equal time width but different amplitudes is that the width of the pulse can be chosen in such a way that all the levels are located in the same region of the respective programming characteristics. In fact, in this particular case, 1 microsecond is the minimum time required for all the levels to end up in the saturation region of the transient characteristic as can be understood from Figure 4 .

In order to program the EEPROM memory cell according to the MLCS method according to the present invention, the memory cell by preference is erased beforehand. Level 0 as mentioned in table 1, in fact, is the erased state of the EEPROM memory cell according to the preferred embodiment of the present invention. Whereas the VVSSI programming pulses corresponding to logic levels 1, 2, and 3 according to Table 1, shift the threshold voltage of the floating gate of the memory cell by injecting into the floating gate an amount of charges which is proportional to the amplitude of the programming pulse, on the other hand the programming pulse corresponding to logic level 0 does not shift said threshold voltage since the amplitude of such pulse is zero. To erase the EEPROM memory cell according to the preferred embodiment of the present invention a method comprising the following two steps is introduced :

(1) A pre-erase programming pulse is applied to the EEPROM memory cell according to a preferred embodiment of the present invention.

(2) An erase pulse is applied to the EEPROM memory cell. The erase pulse can be applied in differnt ways.

First a method of applying the pre-erase pulse is discussed. In order to minimize the effects of cycling, the electrical field induced stress on the devices should be kept as uniform as possible. Unfortunately in Multilevel memory devices this stress is a function of the data stored in the device. For instance, the stress that is build up in a memory cell that has been programmed ten times to level 3 will be much higher than the stress in another memory cell that has been programmed nine times to level 0 and once to level 1. The non uniform nature of this stress results in non predictable shifts of the read-out currents, which greatly compromise the charge storage level discrimination capability of the memory device. This problem can be overcome by applying an additional write pulse before the erase operation. As can be understood from the transient characteristic of SSI, shown in Figure 4, a 10 microsecond pre-erase programming pulse of the highest voltage (12 Volt), brings all the devices to the same high V_T state before the erase operation, regardless of the initial V_T stored inside the cell.

Second a method of applying an erase pulse to the EEPROM memory device is discussed. the following options can be chosen. Erasure can be accomplished in different ways:

1) Fowler-Nordheim tunneling of electrons from the floating gate towards the drain junction is activated by applying a high negative voltage (-10 to -12V) to the program gate, while the supply voltage (5 Volt) is applied to the drain. In this erase mode, the control gate has to be kept grounded in order to maximize the tunneling field at the drain-to-floating-gate overlap. The potential applied to the source junction is of no importance during erasure.

2) If the wordline and the program line of a sector of the memory device are connected during the erase operation, a lower gate voltage can suffice (typically -7 to -8V). The parasitic control-gate-to-floating-gate capacitance is then used to further enhance the electric filed across the tunnel oxide. In this case, the erase mechanism stays essentially the same as in the previous case, but the necessary negative voltage is lowered at the expense of additional switching circuitry.

3) Another possible erase scheme is offered by the channel erase mechanism. In this case a negative voltage is applied to the program line, eventually combined with the supply voltage and applied to the substrate (or p-well) of the memory array. In this case a uniform erase current is obtained in the tunnel oxide region which is beneficial from the point of view of oxide stress and programming window closure after write/erase cycling. The main advantage of this scheme is the absence of any band-to-band tunneling current from the drain junction to the substrate or well.

4) A last possible erase mechanism is the polyoxide conduction from floating gate to control gate which can be established by applying a high positive voltage to the control gate. This is possible without any changes to the cell design. This erase scheme has also been described in US 5583810.

The possible erase modes are summarized in table 2.

	source	drain	control gate	program gate	substrate or p-well
write	0 V	3.3 V/5 V	1 V/1.5 V	12 V	0 V
tunnel erase	-	3.3 V/5 V	0 V	-12 V	0 V
tunnel erase (alternative)	-	3.3 V/5 V	-7 V	-7 V	0 V
channel erase	3.3 V/5 V	3.3 V/5 V	0 V	-12 V	3.3 V/5 V
channel erase (alternative)	3.3 V/5 V	3.3 V/5 V	-7 V	-7 V	3.3 V/5 V
polyoxide erase	-	0 V	12 V	0 V	0 V

Table 2 : Typical operating voltages for the memory cell in a SSI write mode, and the different erase modes.

Read-out Architecture

The prior art multilevel memory devices rely on a parallel architecture for reading out the information stored in the memeory cell similar to the one shown in Fig 5. The memory cell read out current I_C is compared in parallel with three reference currents, which are chosen as the average of the currents corresponding to two adjacent logic levels. Each comparator 37 produces a binary output that is fed to a decoder 38 from which the 2 bits of information are obtained. Due to the considerable area cost of the comparators 37, this architecture extensively increases the periphery of the memory device. In fact, while the comparator utilized to distinguish between 0's and 1's is simple and small (1 bit resolution) in binary memories, the comparators in MLCS memory devices need to be much more accurate (8 bits resolution) and, therefore, consume much more area. Furthermore, this architecture is based on the assumption that regardless of wafer distributions of the read out current, process variations, disturbs and cycling, the read out current corresponding to level 'i' will always be larger than reference 'i' and smaller than reference 'i-1'. When

this not the case, a comparator would switch, leading to an error in identifying the stored charge level. Such assumption can be made only if programming is achieved utilizing program verify techniques. Since the VVSSI programmation method is fitted of not utilizing program verification, a new custom designed architecture has been developed.

In order to minimize the influence of process variations and cycling, four dummy cells D_0, D1, D2 and D3 are provided on each row of the memory array described above. These dummy cells are programmed to level 0,1, 2 and 3 respectively, as explained in Table 1, and are utilized as references during the read-out operation.

When a memory cell 10 is read-out, its read-out current and the currents of the dummy cells D0, D1, D2 and D3 on that row are sensed in parallel. How to implement the sensing device is well known in the art. The read-out current of the memory cell I_{dc} is then compared with each of the currents I_{dx} of the dummy cells to decide to which of the four charge storage levels (0, 1, 2, 3) it belongs. A dedicated circuit has been implemented to carry out these comparisons in parallel in order to reduce the access time. The circuit working principle and block diagram are shown in Figures 6 and 7, respectively. In order to realize the multilevel signal comparison, the distance between the read-out current and each of the currents of the dummy cells is measured by the four subcircuits 400, 401, 402 and 403 of Fig. 7. Each of these produce an intermediate output voltage that is proportional to the similarity of the measured currents: this intermediate output voltage is labeled as the Matching-Score signal (MS). The four MS's are fed to the second stage 500 of the circuit of Fig. 6. This sub-block (500) decides which of the four MS's is the highest and brings the corresponding output terminal (600, 601, 602 or 603) to the high digital state, while the other three outputs remain at the low digital state. The high digital state corresponds to a

voltage equal to the power supply voltage, while the low digital state corresonds to ground.

By means of example the subcircuit 400 is described herebelow. The other subcircuits 401, 402 and 403 are similar to 400. The subcircuits 400, 401, 402 and 403 receive two current input signals I_C and I_X and deliver an intermediate voltage output signal V_{MS} that is proportional to the similarity between the two input currents, that is in this preferred embodiment of the invention the smaller the Euclidean distance between the currents, the higher V_{MS}. The monodimensional Euclidean Distance, as known in the art, can be expressed as:

$$Dist = \sqrt{(R-L)^2} \qquad (1)$$

where R and L are two generic monodimentional vectors, and V_{MS} is a monotonically decreasing function of *Dist*. In order to implement expression (1) on silicon, the intrinsic square law of a long channel MOSFET in saturation is exploited:

$$I_M \equiv K(V_G - V_S - V_T)^2 \qquad (2)$$

Applying a voltage signal (R) to the gate of a MOS is straightforward and known in the art. However, in order to apply a voltage (L) to its source, a second MOSFET in source follower configuration must be connected to the source of the driving n-MOS device. In this way the expression $(R-L)^2$ is implemented. The so obtained current I_M is then fed to a p-MOS device in diode configuration which implements the square root function.

These considerations lead to the sub-circuit shown in Fig. 8, which includes two driving n-MOS device 43, 44 comprising a couple of first driving metal-oxide-semiconductor transistors with the respective source followers 45, 42 comprising a couple of second metal-oxide-semiconductor transistors, a diode connected p-MOS device 47 comprising a third metal-oxide-semiconductor transistor and two current-to-voltage converter n-MOS device 46, 41.

One electrode, i. e. source or drain, of each of said second metal-oxide-semiconductor transistors is connected to one electrode, i. e. source or drain, of one of said first driving metal-oxide-semiconductor transistors. Thereby one of said first driving metal-oxide-semiconductor transistors is connected to one of said second metal-oxide-semiconductor transistors. The gates of said first driving metal-oxide-semiconductor transistors and said second metal-oxide-semiconductor transistors thereby are configured in a cross-like configuration. Thereto the gate of each of said first driving metal-oxide-semiconductor transistors is connected to the gate of one of said second metal-oxide-semiconductor transistors, the second metal-oxide-semiconductor transistor being the one that is not connected with one electrode of said first driving metal-oxide-semiconductor transistor. The third metal-oxide-semiconductor transistor is connected to another electrode, i. e. source or drain, of said first driving metal-oxide-semiconductor transistors, said another electrodes of said first driving metal-oxide-semiconductor transistors being connected.

The dimensions of the transistors are given in the figure as well. 42 and 45 have an aspect ratio W/L which can be from about 5 to about 50 times that of 43 and 44 since these are source follower transistors utilized to bias the source of the driving transistors. However, the wider the source followers with respect to the driving transistor, the more accurately the source follows the gate. Simulations show

that a factor of 10 is a good compromise between accuracy and area consumption.

The transistors 46 and 41 convert I_C and I_X into V_C and V_D respectively. If I_C is larger than I_X, then 44 is cut off since the voltage at its source V_C is higher than the voltage V_D at its gate. However, 43 is on and the larger the difference between V_C and V_D, the larger its drain current, the smaller V_{MS}. On the contrary, if I_C is smaller than I_X then 43 is cut off and 44 is on.

Fig. 9 shows the proposed sub-circuit 500 according to a preferred embodiment of the invention which comprises 4 current n-MOS conveyors 50, 51, 52 and 53 comprising transistors and 4 current comparators 56, 57, 58 and 59. The sub-circuit receives the four V_{MS} 's from the dummy cells D0, D1, D2, D3 as input signals at the gates of the current conveyors and delivers four binary output signals. The current conveyors have the source node X in common and are biased by the same biasing current I_B. When the V_{MS} 's are applied to the gates of the conveyors, node X follows the largest input voltage, turning off the other three conveyors: the biasing current will flow only through the conveyor with the largest V_{MS}. Only the conveyor with the largest V_{MS} will drive current, while the other three conveyors will not. The drain of each of the conveyors is connected to the drain of transistor 54 of the current comparator which is on top of the conveyor. The current comparator, that is implemented according to principles known in the art, compares the current coming from the conveyor with the bias current I_B /2. If the current coming from the conveyor is larger than I_B /2, then the output of the comparator will be high. If, on the contrary, the current coming from the conveyor is smaller than the bias current I_B /2, then the output of the comparator will be low. Since the current I_B flows almost entirely in one and only one of the conveyors, it follows that one and only one of the current comparators will set its output to the high digital state, while the other three

current comparators will set their output to the low digital state.

The circuit has been integrated in a standard double-polysilicon double-metal 0.7-μm process with a silicon area of only 140 x 100 μm^2, as shown in the picture of Fig. 10, and has been extensively evaluated. The silicon area for implementing a single 8-bit comparator is estimated to be around 70 x 50 μm^2. Since 3 comparators are needed, the classical architecture of Fig. 5 would take at least 210 x 150 μm^2 of silicon area and would result in a 'level identifying' block almost 2.3 times larger than the one proposed according to this invention. For power consumption in the same range, they show comparable propagation delay. However, in the circuit proposed here it is possible to significantly decrease the propagation delay simply by increasing the circuit biasing currents. This is not so straightforward in standard comparators where an increase of the biasing current would result in larger offset voltage and lower accuracy. The speed of the read-out and 'level identifying' circuitry significantly influences the data throughput of the memory due to the program verify schemes that are normally utilized in MLCS.

Fig. 11 shows the experimentally evaluated V_{MS} as a function of a sweeping cell current in the case of a reference current of 25 μA; as expected, the better the current match, the higher V_{MS}. Fig. 12 shows the experimental output voltages of the read-out circuit as a function of a sweeping cell current in the case of reference currents of 30, 80, 120 and 160 μA. Only one output voltage is high for any given cell current value.

Each time the memory device is flash erased, for instance before a write operation, the dummy cells belonging to that particular sector are erased as well and reprogrammed to the reference levels. This technique ensures that both the dummy and the memory cells experience the very same duty

cycle and, therefore, the same current shifts. This means that the overall shift due to cycling cancels out when comparing dummies and memory cells during read-out. Repeating the dummy cells on each wordline eliminates another effect that plays an important role in high density memories: the drain resistance effect. Due to the resistive nature of the drain line there is a difference in the read-out currents of the cells belonging to the same column. This difference, although negligible for memory cells close to each other, could become quite large for spaced-apart cells and should not be taken into account if the dummy cells are not on the same row as the cell to be read-out. The additional cost in terms of silicon area of such an architecture is very limited since it comprises only four cells per wordline.

WHAT IS CLAIMED IS :

1.
A memory device adapted for multi-level charge storage comprising:

a plurality of flash eeprom memory cells including a source region, a drain region, a channel region and a floating gate, said floating gate including first and second floating gate portions, said first portion extending over said channel region, said second portion extending away from said channel region, said memory cells further including a program gate and a control gate, said program gate forming a capacitor with said second floating gate portion;

readout means for parallel outputting binary data corresponding to said charge levels stored in said cells; and

programming means for applying a high voltage pulse with a predetermined amplitude, selected from a plurality of predetermined amplitudes and with an essentially fixed time width to said cells, said predetermined amplitudes determining said charge levels.

2.
The memory device according to claim 1 wherein said plurality of memory cells is arranged in an array with rows and columns having :

the drains of the cells belonging to the same column connected together whereby forming a data output line;

the program gates of the cells belonging to the same column connected together whereby forming a data input line; and

the control gates of the cells belonging to the same row connected together whereby forming a word line.

3.
The memory device according to claim 2, wherein said data input line and said data output line are essentially parallel and routed in the same direction; and said word line is

routed in a direction that is essentially perpendicular to the direction of said data input line and said data output line.

4.

The memory device as recited in claim 3 wherein said array further comprises dummy cells on essentially each row of the array, said dummy cells providing reference currents in read-out operation.

5.

A method of storing one of a plurality of charge levels in a memory cell of a memory device adapted for multi-level charge storage, said memory cell including a source region, a drain region, a channel region and a floating gate, said floating gate including first and second floating gate portions, said first portion extending over said channel region, said second portion extending away from said channel region, said memory cell further including a program gate and a control gate, said program gate forming a capacitor with said second floating gate portion, said method comprising the steps of :

applying a low voltage to said control gate;

applying a voltage not greater than 5 Volt to said drain region; and

applying a high voltage pulse with a predetermined amplitude, selected from a plurality of predetermined amplitudes and with an essentially fixed time width to said program gate, said predetermined amplitudes determining said charge levels.

6.

The method as recited in claim 5 further comprising the step of erasing said cell and thereafter executing the steps as recited in claim 4.

7.
The method as recited in claim 6 wherein essentially each memory cell of said device is erased, and wherein said step of erasing said memory cells comprises the steps of :

applying a low voltage to said control gates of essentailly each of said cells of said array;

applying a voltage not greater than 5 Volt on said drain regions of essentialy each of said cells of said array; and

applying a high voltage pulse with a predetermined amplitude and an essentially fixed time width on said program gates of essentailly each of said cells of said array;

and thereafter executing the steps as recited in claim 6.

8.
The method as recited in claim 5 wherein said high voltage pulse is capacitively coupled to said second floating gate portion, thereby causing a hot-electron injection towards said floating gate whereby the charge level is stored in said memory cell.

9.
The method as recited in claim 8 wherein said memory cell is implemented in a 0.7 µm CMOS technology, said low voltage is smaller than or equal to 1.5 Volt and said high voltage pulse being selected form the predetermined amplitudes 12 Volt, 8 Volt, or 7 Volt, and 0 Volt said width being about 1 microsecond.

10.
A method of reading out the charge level of a memory cell of a memory device, said cell comprising a cell having a source region, a drain region, a channel region and a floating gate, said floating gate including first and second floating gate portions, said first portion extending over said channel region, said second portion extending away from said channel region, said memory cell further including a program gate and

a control gate, said program gate forming a capacitor with said second floating gate portion, said method comprising the steps of :

sensing the drain current of said memory cell;

sensing the drain currents of a plurality of dummy cells;

measuring the similarities between said drain current of said memory cell
and said drain currents of said plurality of dummy cells whereby obtaining a plurality of intermediate voltages representing said similarities;

determining the highest among said intermediate voltages whereby identifying the dummy cell having the drain current closest to the drain current of said memory cell;

setting a predetermined voltage on one of a plurality of output terminals, said one output terminal corresponding to said dummy cell having the drain current closest to the drain current of said memory cell.

11.

An apparatus for reading out the charge level of a memory cell of a memory device, said memory cell including a source region, a drain region, a channel region and a floating gate, said floating gate including first and second floating gate portions, said first portion extending over said channel region, said second portion extending away from said channel region, said memory cell further including a program gate and a control gate, said program gate forming a capacitor with said second floating gate portion, the apparatus comprising :

a plurality of dummy cells for delivering a plurality of reference currents ;

means for reading out said reference currents and the current of said memory cell;

a plurality of analogue circuits for measuring the similarity between said current of said memory cell and each of said reference currents whereby outputting a plurality of intermediate voltages representing said similarities;

a decision circuit for determining the highest among said intermediate voltages whereby determining the dummy cell having the drain current with the smallest distance from the drain current of said memory cell and for setting a predetermined voltage on one of a plurality of output terminals, said one output terminal corresponding to said dummy cell having the drain current with the smallest distance from the drain current of said memory cell.

12.
The apparatus as recited in claim 11 wherein said similarity is measured as the Euclidean distance between said current of said memory cell and each of said reference currents.

13.
The apparatus as recited in claim 12 wherein said analogue circuits comprise a long channel metal-oxide-semiconductor transistor.

14.
The apparatus as recited in claim 12 wherein said analogue circuits comprise:

a couple of first driving metal-oxide-semiconductor transistors;

a couple of second metal-oxide-semiconductor transistors, one electrode of each of said second metal-oxide-semiconductor transistors being connected to one electrode of one of said first driving metal-oxide-semiconductor transistors, one of said first driving metal-oxide-semiconductor transistors thereby being connected to one of said second metal-oxide-semiconductor transistors, the gate of each of said first driving metal-oxide-semiconductor transistors being connected to the gate of one of said second metal-oxide-semiconductor transistors, the second metal-oxide-semiconductor transistor being the one that is not connected with one electrode of said first driving metal-oxide-semiconductor transistors, the gates of said first

driving metal-oxide-semiconductor transistors and said second metal-oxide-semiconductor transistors thereby being configured in a cross-like configuration; and

a third metal-oxide-semiconductor transistor being connected to another electrode of said first driving metal-oxide-semiconductor transistors, said another electrodes of said first driving metal-oxide-semiconductor transistors being connected.

15.
The apparatus as recited in claim 14 wherein the gate of said third metal-oxide-semiconductor transistor is short-circuited with the electrode of said third metal-oxide-semiconductor transistor that is connected to said first metal-oxide-semiconductor transistors.

16.
The apparatus as recited in claim 15 wherein said first driving metal-oxide-semiconductor transistors are n-MOS transistors, said one electrode being the source of said first driving metal-oxide-semiconductor transistors, and said other electrode of said first driving metal-oxide-semiconductor transistors being the drain of said first driving metal-oxide-semiconductor transistors, said third metal-oxide-semiconductor transistor being a p-MOS transistor.

17.
The apparatus as recited in claim 14 wherein said second metal-oxide semiconductor transistors have an aspect ratio W/L which is about 10 times the aspect ratio W/L of said first metal-oxide-semiconductor transistors.

18.
The apparatus as recited in claim 11 wherein said decision circuit comprises a plurality of current conveyor transistors and current comparators, said current conveyors having one

electrode being connected to the same current biasing source, the gate electrode of said current conveyors being modulated by said intermediate voltages.

5

FIG 1

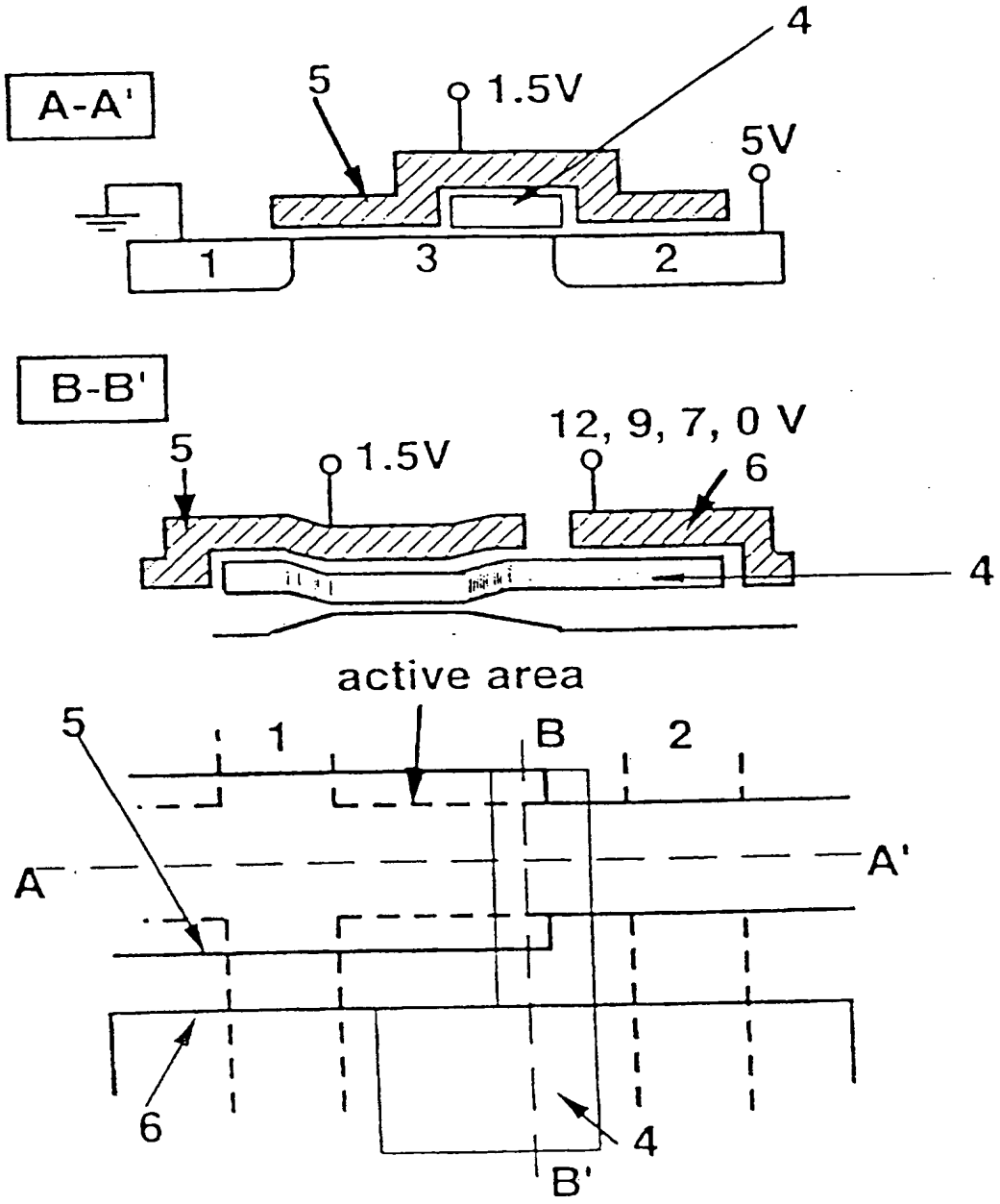


FIG 2

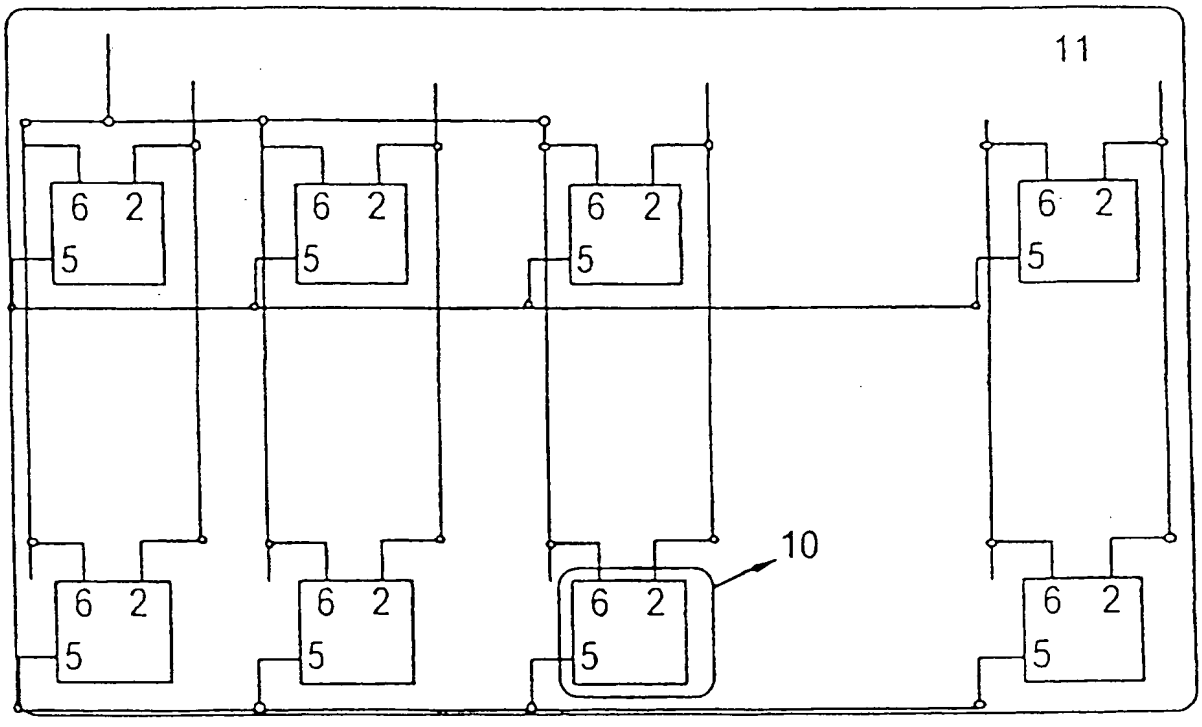
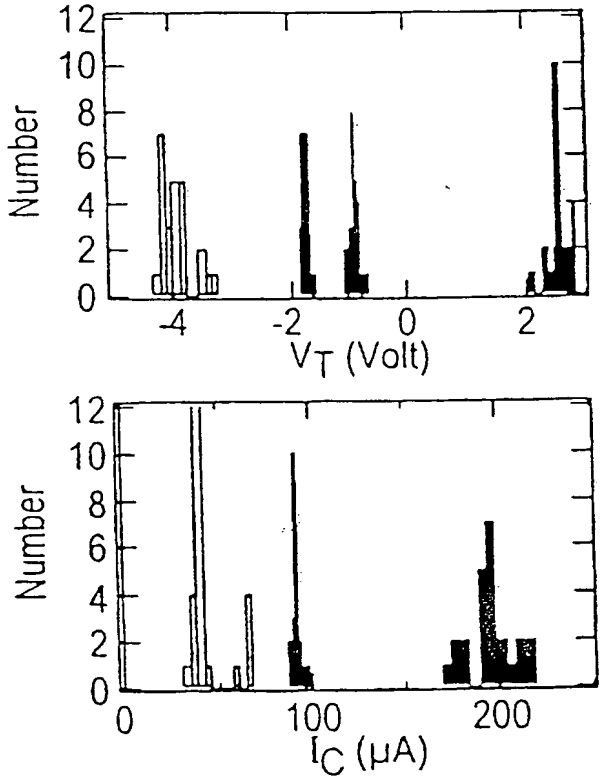


FIG 3



	V_T (V)		I_D (μA)	
Level	X	σ	X	σ
0	-3.92	0.27	195	12
1	-1.72	0.06	91	2
2	-0.89	0.09	43	9
3	2.60	0.18	0	0

FIG 4

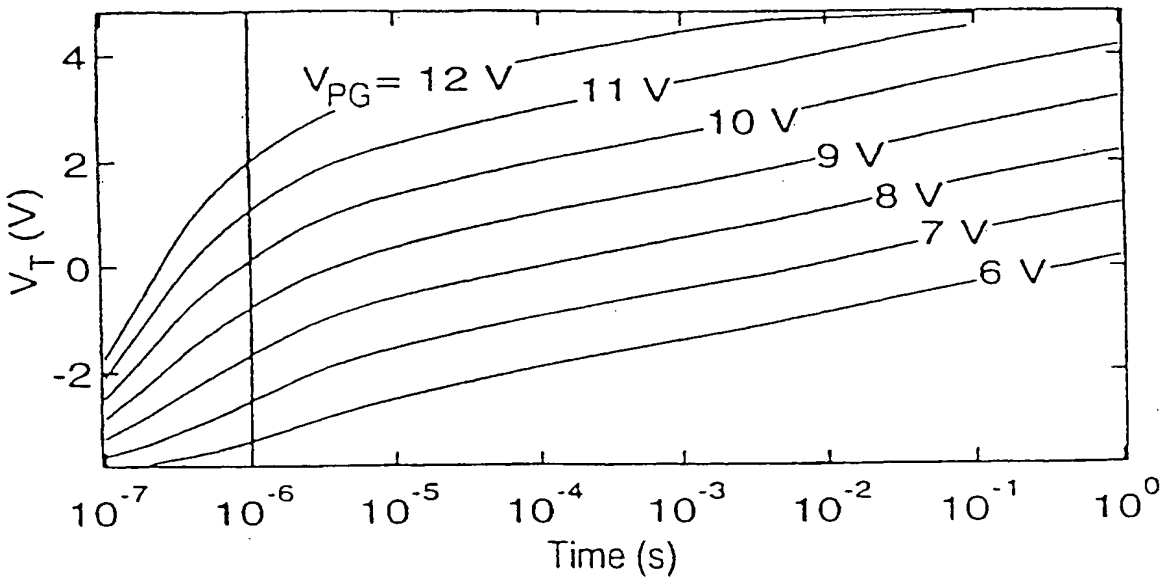

4
2
0
-2
V_T (V)
V_{PG}= 12 V
11 V
10 V
9 V
8 V
7 V
6 V
10^{-7}
10^{-6}
10^{-5}
10^{-4}
10^{-3}
10^{-2}
10^{-1}
10^{0}
Time (s)

FIG 5

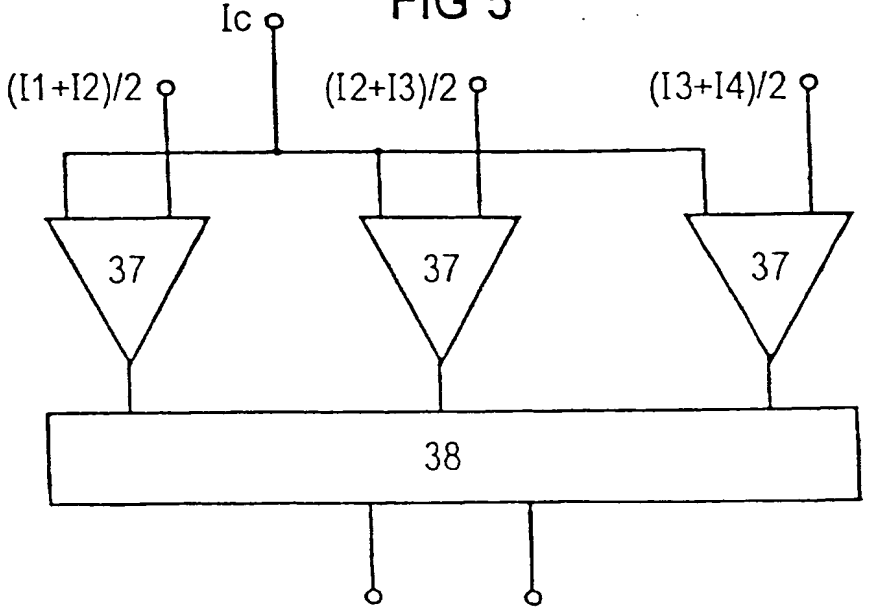

Ic
(I1+I2)/2
(I2+I3)/2
(I3+I4)/2
37
37
37
38

FIG 6

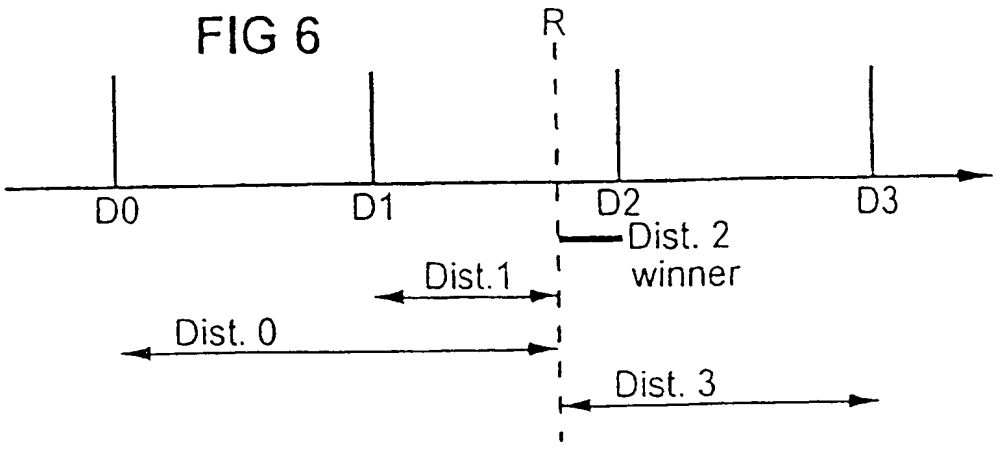

R
D0
D1
D2
D3
Dist. 2
winner
Dist.1
Dist. 0
Dist. 3

FIG 7

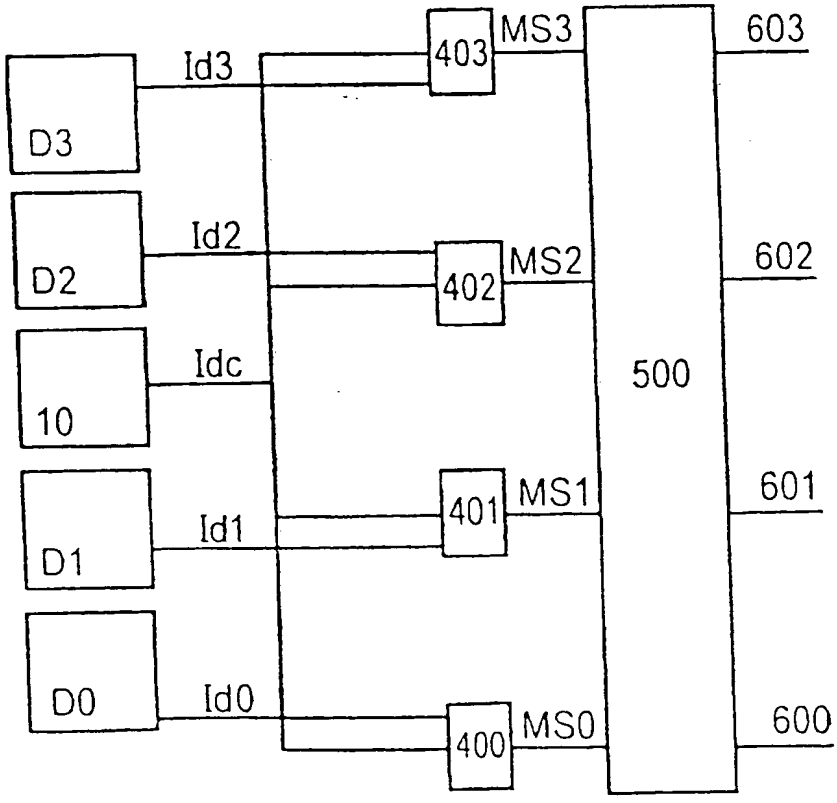

D3
Id3
403
MS3
603
D2
Id2
402
MS2
602
10
Idc
500
D1
Id1
401
MS1
601
D0
Id0
400
MS0
600

FIG 8

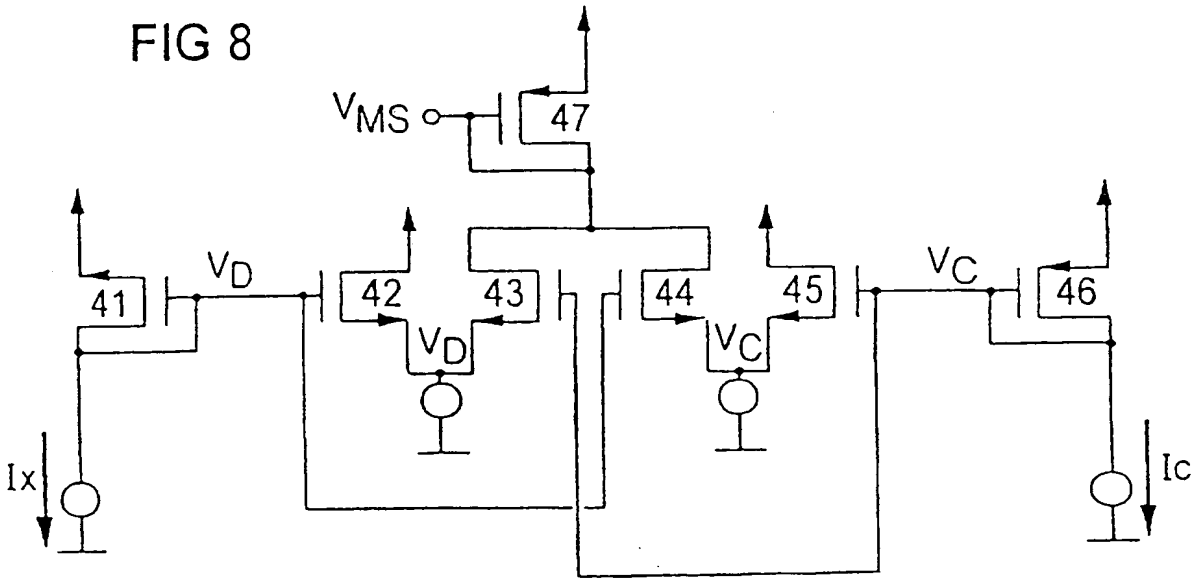

VMS
47
VD
41
42
43
VD
44
45
VC
VC
46
Ix
Ic

FIG 9

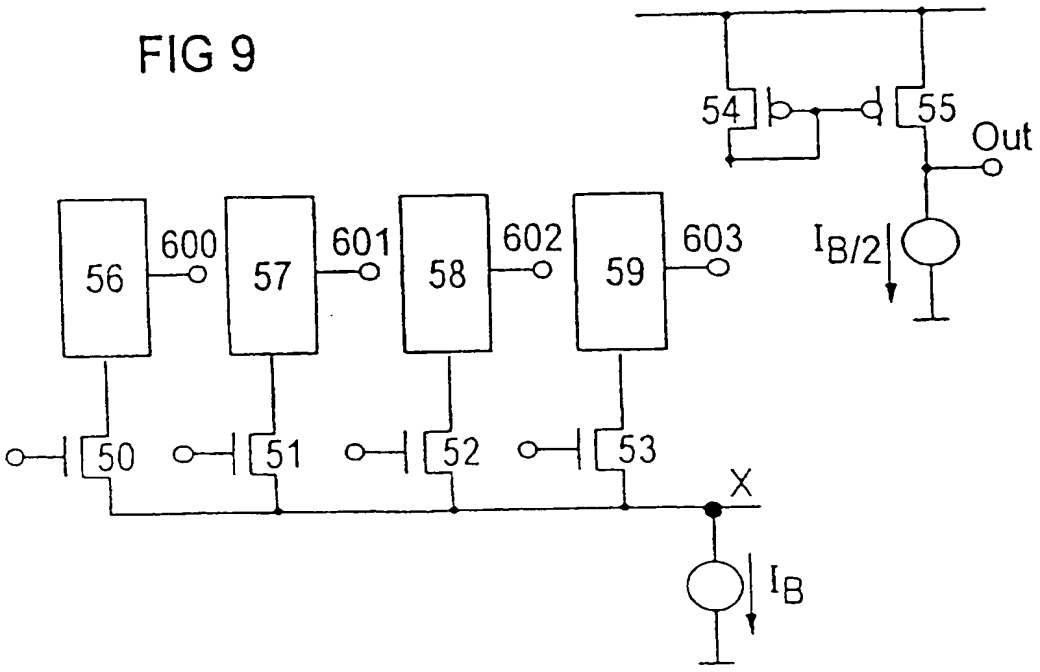

54
55
Out
56
600
57
601
58
602
59
603
IB/2
50
51
52
53
X
IB

FIG 10

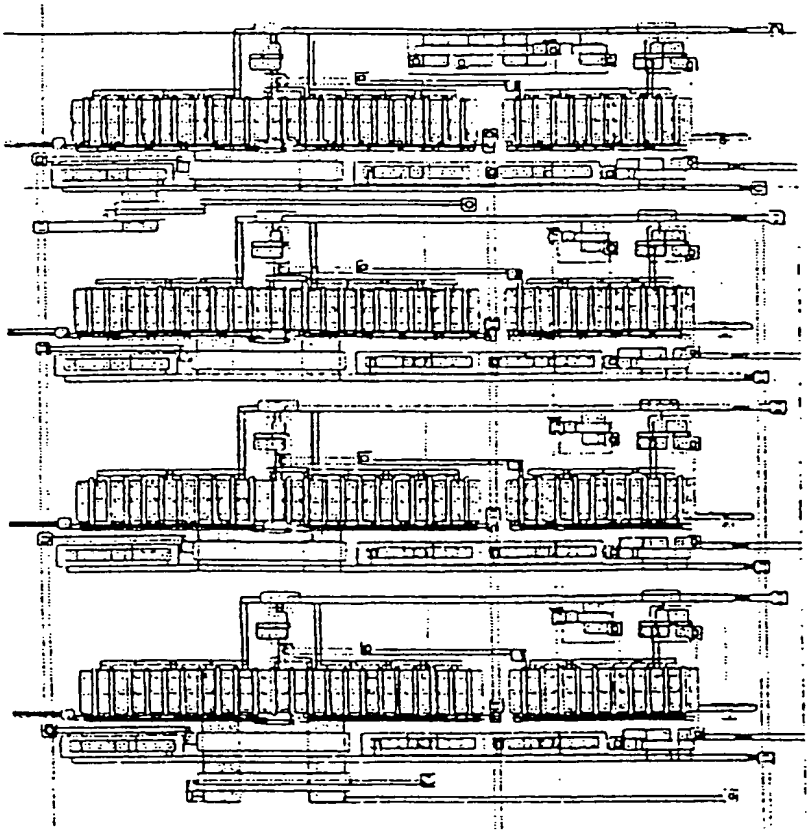


FIG 11

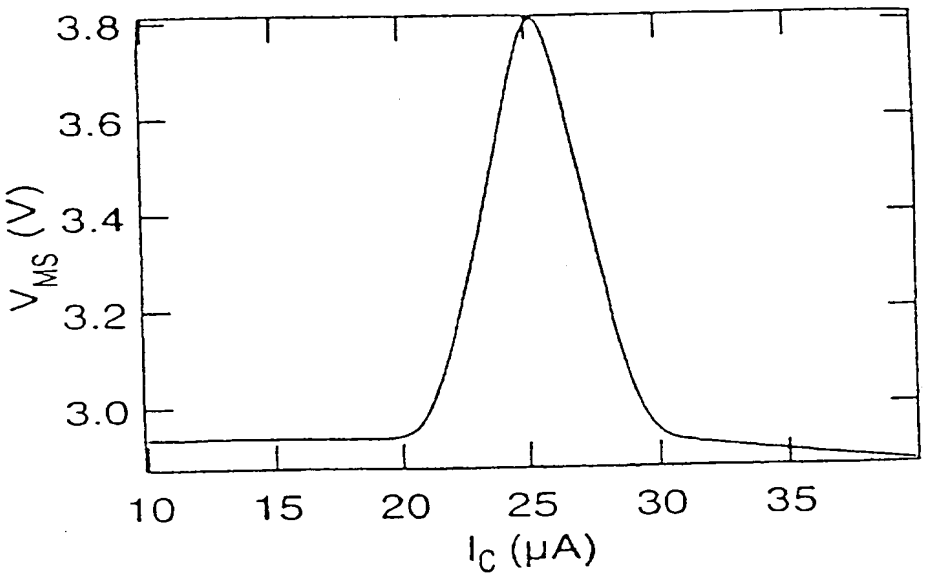
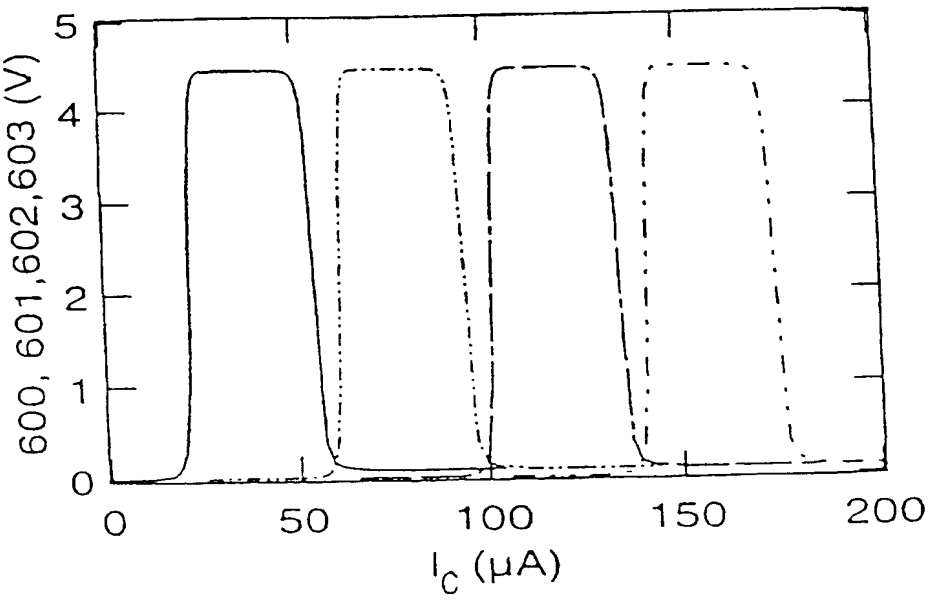

3.8
3.6
3.4
3.2
3.0
V_{MS} (V)
10
15
20
25
30
35
I_C (μA)

FIG 12


5
4
3
2
1
0
600, 601,602,603 (V)
0
50
100
150
200
I_C (μA)

INTERNATIONAL SEARCH REPORT

International Application No
PCT/EP 97/00561

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G11C11/56

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G11C

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 4 649 520 A (EITAN) 10 March 1987 see column 2, line 25 - column 4, line 31; figures 1,2	1,5,10
P,Y	EP 0 756 287 A (SANDISK CORPORATION) 29 January 1997 see page 7, column 12, line 8 - page 10, column 18, line 24; figures 7-9	1,10
Y A	US 5 418 743 A (TOMIOKA ET AL) 23 May 1995 see column 4, line 1 - column 4, line 49	1,5 4
A	EP 0 501 941 A (INTERUNIVERSITAIR MIKROELEKTRONICA CENTRUM) 2 September 1992 cited in the application see the whole document	1-3,6-9

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 October 1997	20. 11. 97

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Degraeve, L

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Inter...ional Application No
PCT/EP 97/00561

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US 4 616 245 A (TOPICH ET AL) 7 October 1986 see the whole document	1
A	US 4 532 535 A (GERBER ET AL) 30 July 1985 see column 5, line 13 - column 6, line 39; figures 1,2	1
A	US 5 163 021 A (MEHROTA ET AL) 10 November 1992 see column 9, line 38 - column 12, line 35; figures 7A,7B,9	11,13,14
A	US 4 670 675 A (DONOGHUE) 2 June 1987 see the whole document	11,14
A	WO 93 25005 A (INDIANA UNIVERSITY FOUNDATION) 9 December 1993 see page 8, line 1 - page 12, line 22; figures 1-9	
A	ETIEMBLE ET AL: "CONCEPTION AVEC RÈGLES EN LAMBDA D'UNE ROM 4-VALUÉE" REVUE DE PHYSIQUE APPLIQUEE., vol. 20, no. 2, February 1985, PARIS FR, pages 71-75, XP002045165 see page 72, column 2, line 1 - page 73, column 2, line 19; figure 3	14
A	US 5 298 808 A (TERRELL) 29 March 1994 see the whole document	11

4

INTERNATIONAL SEARCH REPORT

'ernational application No.
PCT/EP 97/00561

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This International Search Report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the International Application that do not comply with the prescribed requirements to such an extent that no meaningful International Search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of Invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see annexed sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this International Search Report covers all searchable claims.

2. ☐ As all searchable claims could be searched without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this International Search Report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this International Search Report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/210

1. Claims 1-10 : Extended floatiing gate EEPROM cells with parallel readout & programming during a fixed period with a voltage selected among a plurality of programming.

2. Claims 11-18: A readout circuit for an extended floating gate EEPROM cell, using analogue circuitry for determining a read current which is the closest to a reference current among a plurality of reference currents.

INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter. ..ional Application No
PCT/EP 97/00561

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